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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,158	03/19/2004	Yoshi Ono	SLA0830	8642

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EXAMINER	
PIZARRO CRESPO, MARCOS D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/805,158	ONO ET AL.	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16,17 and 20-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16,17 and 20-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Attorney's Docket Number: SLA0830
Filing Date: 3/19/2004
Claimed Foreign Priority Date: none
Applicant(s): Ono et al.
Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the response and declaration filed on 8/2/2006.

Acknowledgment

1. The response and declaration both filed on 8/2/2005 in response to the Office action mailed on 3/10/2006 have been entered. The present Office action is made with all the presented arguments being fully considered. Accordingly, pending in this Office action are claims 16, 17, and 20-28.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 16, 17, 20-22, and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halliyal (US 6451641) in view of King (US 6754104) and Kirkpatrick (US 4197144).

5. Regarding claim 16, Halliyal shows most aspects of the instant invention including a method of fabricating a non-volatile memory transistor comprising the steps of:

- ✓ Preparing a semiconductor substrate (see, *e.g.*, fig. 5/step S501)
- ✓ Forming a gate stack on the substrate as follows:
  - Depositing a single layer of high-k dielectric material, without an underlying oxide insulator layer and an overlying oxide insulator layer (see, *e.g.*, fig. 5/step S502)
  - Forming an electrode layer overlying the dielectric material (see, *e.g.*, fig. 5/step S503)
- ✓ Forming drain and source regions **104/106** on opposite sides of the gate stack (see, *e.g.*, fig. 1)

Halliyal, however, fails to show the step of inducing trapping centers in the dielectric material in response to an ionized species exposure. King (see, *e.g.*, col.14/ll.16-20), on the other hand, teaches that implanting impurity atoms into Halliyal's

dielectric material layer would form a charge-trapping region within the layer. This, according to Kirkpatrick (see, *e.g.*, col.4/ll.5), would increase the number of storage sites within Halliyal's dielectric layer.

It would have been obvious at the time of the invention to one of ordinary skill in the art to induce trapping centers into the dielectric material by exposing the dielectric to an ionized species, as suggested by King and Kirkpatrick, to increase the number of storage sites within the dielectric layer.

6. Regarding claim 17, Halliyal shows the high-K dielectric material comprising hafnium oxide (see, *e.g.*, col.6/ll.37).

7. Regarding claim 20, King shows the ionized species including nitrogen (see, *e.g.*, col.3/ll.56).

8. Regarding claim 21, Halliyal/King/Kirkpatrick show most aspects of the instant invention (see, *e.g.*, paragraph 5 above). King (see, *e.g.*, col.6/ll.3) and Kirkpatrick (see, *e.g.*, col.4/ll.3) also teach performing the step of inducing trapping centers in the dielectric by exposing the dielectric to plasma to incorporate the trapping sites into the layer. Halliyal/King/Kirkpatrick, however, fail to specify an exposure time of about 10-100 seconds. Although they fail to specify the time of duration of the plasma exposure, performing King/Kirkpatrick's step would necessarily require a certain amount of time. The specification, on the other hand, fails to teach about the criticality of having a specific plasma exposure time of 10-100 seconds. It has been held that time differences will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such time is critical. "Where the general

conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation". *In re Aller*, 220 F.2d 454,456,105 USPQ 233, 235 (CCPA 1955).

Since the applicants have not established the criticality (see next paragraph) of the exposure time claimed, it would have been obvious to one of ordinary skill in the art to use these values in the method of Halliyal/King/Kirkpatrick.

CRITICALITY

9. The specification contains no disclosure of either the critical nature of the claimed exposure time or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

10. Regarding claim 22, Halliyal shows the trapping layer is deposited by an ALD method (see, *e.g.*, col.6/ll.33).

11. Regarding claim 25, Halliyal shows the substrate is an SOI substrate (see, *e.g.*, col.5/ll.66).

12. Regarding claim 26, Halliyal shows the transistor is a multi-bit transistor (see, *e.g.*, col.5/ll.20).

13. Regarding claim 27, Kirkpatrick uses an ion energy in the range of 10 to 300 keV and a dose in the range of about $1x10^{14}$ to $1x10^{17}$ for the step of exposing the dielectric material (see, *e.g.*, col.3/ll.56 and col.4/ll.26).

14. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Halliyal/King/Kirkpatrick in view of Chooi (US 6486080) and Agarwal (US 2001/0015453).

15. Regarding claim 23, Halliyal/King/Kirkpatrick show most aspects of the instant invention (see, *e.g.*, paragraph 5 above), except for a densification anneal step after depositing the charge-trapping layer. Chooi (see, *e.g.*, col.6/ll.5-7) and Agarwal (see, *e.g.*, par.0005/ll.5-10), on the other hand, suggest following Halliyal's trapping layer deposition with an anneal step to densify the layer. This densification step would fill any oxygen vacancies developed in the layer during its formation.

It would have been obvious at the time of the invention to one of ordinary skill in the art to follow the deposition step of Halliyal/King/Kirkpatrick's trapping layer with the anneal step suggested by Chooi and Agarwal to cure oxygen vacancies developed in the layer during the deposition step.

16. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Halliyal/King/Kirkpatrick in view of Liang (US 5372957).

17. Regarding claim 24, Halliyal/King/Kirkpatrick show most aspects of the instant invention (see, *e.g.*, paragraph 5 above) except for the formation of the drain and source regions comprising an angle source/drain implantation. Liang (see, *e.g.*, col.5/ll.4-7), on the other hand, teaches that angle implantation would place the ions further into the gate region of Halliyal's transistor without driving in the dopants. The resultant structure would be more immune to hot carrier degradation.

It would have been obvious at the time of the invention to one of ordinary skill in the art to form Halliyal/King/Kirkpatrick's source/drain regions using the angle implantation suggested by Liang to protect the transistor against hot carrier degradation.

18. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Halliyal/King/Kirkpatrick in view of Moslehi (US 5372957).

19. Regarding claim 28, Halliyal/King/Kirkpatrick show most aspects of the instant invention (see, *e.g.*, paragraph 5 above). King (see, *e.g.*, col.6/ll.37) and Kirkpatrick (see, *e.g.*, col.4/ll.3) also teach the step of exposing the dielectric includes generating plasma. They, however, fail to show that generating the plasma includes using an inductively coupled plasma (ICP) source. Moslehi, on the other hand, suggests using an ICP source over other conventional plasma sources due to its superior process performance, throughput rate, and control capabilities including its ability to control the plasma density and ion energy independent of each other (see, *e.g.*, col.1/ll.30-64).

It would have been obvious at the time of the invention to one of ordinary skill in the art to use an ICP source to generate the plasma of Halliyal/King/Kirkpatrick, as suggested by Moslehi, because of its superior performance, throughput rate, and control capabilities.

Response to Arguments and Declaration under 37 CFR §1.132

20. The declaration under 37 CFR 1.132 filed on 8/2/2006 is insufficient to overcome the rejection of the claims based upon Halliyal/Kirkpatrick/King as set forth below.

21. The affiant argues:

Halliyal does not describe charge trapping, or the use of a FET as a memory. Halliyal's high-k dielectric cannot store a charge. While King does describe forming charge traps in a gate dielectric, these trap regions have nothing to do with non-volatility. Kirkpatrick describes a PIN diode that can be used as a memory because of charge traps formed in the silicon oxide insulator (I) between the PN junction. The applicants neither describe an insulator between P and N regions, nor a diode memory device.

Of the three primary references, King and Halliyal use high-k dielectrics, but their devices cannot be used for a non-volatile memory. While King describes a high-k dielectric with charge-trapping centers, King's charge trapping centers cannot hold a charge or store a memory state.

In summary, this combination of references does not suggest a memory transistor with a high-k dielectric charge-trapping region.

22. The examiner responds:

It is noted that some of the features upon which the applicants rely (*i.e.*, charge trapping centers that hold a charge or store a memory state) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The recitation "a non-volatile memory transistor" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone, as in the present case. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

In any event, although Halliyal does not describe the use of a FET as a memory, he clearly specifies that his invention is not restricted to the MOSFET illustrated in fig. 1, and may be applied to any semiconductor device in which a high-K gate dielectric and a polysilicon or polysilicon-germanium gate electrode is used, for example, a FET (see, *e.g.*, Halliyal: col.5/ll.12-20). Like Halliyal, King shows a FET in which a high-K gate dielectric and a polysilicon or polysilicon-germanium gate electrode is used. . King

further teaches using Halliyal's FET in a memory cell by incorporating charge traps in the high-k dielectric layer of the transistor (see, *e.g.*, King: fig.1 and col.14/ll.26-22). In this manner a memory circuit can be manufactured that would provide reduced circuit complexity, lower-power operation, and higher-speed operation.

Data can be written or read from King's memory cell in any conventional fashion known to those in the art (see, *e.g.*, King: col.8/ll.56-60). Kirkpatrick, on the other hand, teaches to increase the amount or charge that can be written into King's gate dielectric by increasing the number of defects in the insulator (see, *e.g.*, Kirkpatrick: abstract).

In summary, King teaches uses Halliyal's FET in a memory circuit to provide lower-power operation, and higher-speed operation, whereas Kirkpatrick teaches that King's step of exposing the gate dielectric to an ionized species will increase the defects in the insulator and, consequently, the amount of charge that can be written into the dielectric. Therefore, the combination of references is proper.

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

24. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

25. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(571) 273-8300**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 10:00 AM to 8:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

27. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the

automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

28. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/288,295,310,314,324-326,410,411	9/6/2006
Other Documentation:	
Electronic Database(s): EAST (USPAT, EPO, JPO)	9/6/2006

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